

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of the Claims:

1-4. (canceled)

5. (currently amended) A method for testing a device, comprising:
testing an electronic device having a first operating frequency by a tester device having a second operating frequency;

during the testing, repeatedly determining any frequency difference between the first operating frequency and the second operating frequency; [[and]]

for each determination of the frequency difference, generating a voltage value indicative of the frequency difference; ~~and equalizing the first and the second operating frequencies using the voltage value.~~

using the generated voltage to adjust the first operating frequency.

6-20. (canceled)

21. (new) A testing system for testing a plurality of integrated circuit devices;
comprising

a tester having an operating frequency;

a board adapted to accommodate a plurality of integrated circuit devices to be tested;

a plurality of integrated circuit device under test (DUT) on the board,

a plurality of clock circuits, each generating a operating frequency for a DUT;

a plurality of phase comparator devices affixed on the tester;

each phase comparator device having a pair of input terminals adapted to receiving the operating frequency of the tester and the operating frequency of a DUT, and an output terminal adapted to transmitting a signal indicative of a difference between the operating frequencies of the tester and the DUT; and

TI-36929

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each clock circuit including a voltage controlled oscillator (VCO) circuit operable to adjust the DUT operating frequency based on the output signal of the phase comparator device.

22. (new) The testing system of claim 21, in which the comparator devices are not affixed on the board.

23. (new) The testing system of claim 21, in which a portion of the clock circuit is embedded in the integrated circuit DUT.

24. (new) The testing system of claim 21, in which the comparator is a part of a PLL circuit, which further comprises a low pass filter and an amplifier.

25. (new) The testing system of claim 24, in which the VCO circuit is coupled to the amplifier.

TI-36929